CS152/252A
Fall 2026

Pipelining
Discussion 2

1 Iron Law

1.1 For each term in the Iron Law, give at least three techniques that improve that term.

Instructions/program:

Cycles/instruction:

Time/cycle:

1.2 Explain how each term changes given the proposed modification (increase / decrease / no effect).

(a) [**Quiz 1, 2013**] Remove hardware floating-point instructions (and the pipelined FP-Unit) and instead use software subroutines for floating-point arithmetic

Instructions/program:

Cycles/instruction:

Time/cycle:

(b) [**Sp24 MT1 Q2.2**] Suppose we extended the RISC-V Base ISA with a conditional move instruction which copies `rs1` to `rd` if and only if `rs2` is nonzero.

Instructions/program:

Cycles/instruction:

Time/cycle:

Tip: Iron Law questions might be ambiguous (by design), therefore you must state your assumptions in your answer to receive full credit!

2 Pipeline Hazards

2.1 Define the three types of pipeline hazards.

Data:

Structural:

Control:

2.2 Which type(s) of data hazard is/are possible in a classic RISC-V pipeline?

```
ADD x1, x2, x3
SW  x4, 4(x1)
```
Read-After-Write (RAW)

```
ADD x1, x2, x3
SUB x2, x4, x5
```
Write-After-Read (WAR)

```
ADD x1, x2, x3
SUB x1, x4, x5
```
Write-After-Write (WAW)

2.3 Data Hazards: Identify all potential hazards

```
ADDI   x1, x0, 4
SW     x1, 8(x2)
SLLI   x3, x1, 1
ADD    x2, x1, x3
LW     x1, 0(x3)
SUB    x1, x0, x0
```

RAW	WAR	WAW
`addi -> sw`	`sw <- add`	`addi -> lw`

2.4 Structural Hazards

(a) Are there any structural hazards in a classic 5-stage RISC pipeline?

(b) Are there any structural hazards in the single-bus microcoded machine?

(c) What modifications to a RISC pipeline may introduce a structural hazard?

3 Data Hazard Mitigations

3.1 From lecture, what are the two strategies for handling data hazards?

Interlock:

Bypass:

Consider the following linked-list traversal program. For the pipeline diagrams below, assume:

(a) The register file is write-through (an instruction in D can read the value being written back in W in the same cycle)
(b) Branches are always predicted taken; squash if wrong
(c) Memory is always single cycle
(d) The loop runs for 2 iterations

```
      ADDI  x2, x0, 0x700
LOOP: ADD   x1, x2, x0
      LW    x2, 4(x2)
      BNE   x2, x0, LOOP
      SW    x3, 4(x1)
```

Case 1: Interlock

3.2 Identify the hazards.

3.3 Fill out the pipeline diagram for the interlocked pipeline (no bypassing).

```
      ADDI  x2, x0, 0x700
LOOP: ADD   x1, x2, x0
      LW    x2, 4(x2)
      BNE   x2, x0, LOOP
      SW    x3, 4(x1)
```

Case 1: Interlock pipeline

3.1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
addi																														
(1) add																														
lw																														
bne																														

3.4 Interlock questions

- How many bubbles were needed?

- What is the CPI for this program with interlocking? (CPI is measured from when the first instruction commits to when the last instruction in the sequence commits.)

- What is the CPI assuming branches are always predicted correctly?

3.5 Interlocking & Iron Law. [**Quiz 1, 2011**] In a classic RISC pipeline, modify the ISA (and thus the microarchitecture) to use hardware interlocking instead of software interlocking for both branch delay slots and load-use delay slots.

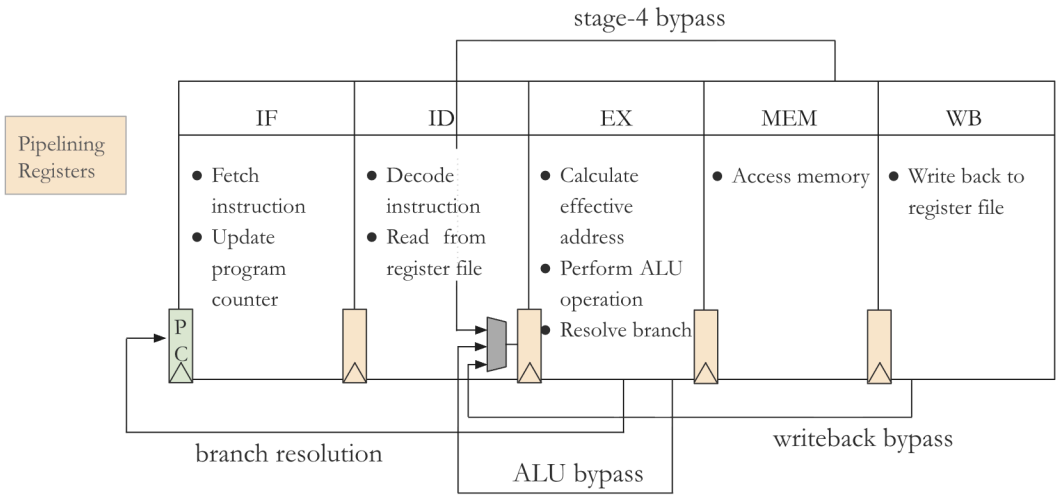
What is software interlocking?

Instructions/program:

Cycles/instruction:

Time/cycle:

Case 2: Bypass



3.6 Using the same code and assumptions, fill out the pipeline diagram for the bypassed pipeline shown above (ALU bypass, stage-4 bypass, and writeback bypass).

```
      ADDI  x2, x0, 0x700
LOOP: ADD   x1, x2, x0
      LW    x2, 4(x2)
      BNE   x2, x0, LOOP
      SW    x3, 4(x1)
```

Case 2: Bypass pipeline

3.3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
addi																														
(1) add																														
lw																														
bne																														

3.7 Bypass questions

- What is the CPI with bypass?

- What is the CPI if load accesses take 2 cycles?

- What is the CPI assuming branches are always predicted correctly?