

1 Tomasulo's Algorithm

Recall from last week that a naive out-of-order pipeline is bottlenecked by WAR and WAW hazards. These are *false* dependencies: they come from reusing a small set of architectural registers, and would not exist if we had an unlimited number of registers. **Register renaming** removes them by mapping each new write of an architectural register to a different physical register.

Original code:

A: fmul f1, f0, f2
B: fadd f0, f3, f1
C: fmul f3, f2, f3
D: fadd f3, f3, f1

Renamed code:

A: fmul P4, P0, P2
B: fadd P5, P3, P4
C: fmul P6, P2, P3
D: fadd P7, P6, P4

Rename table		
	Initial	Updated
f0	P0	P5
f1	P1	P4
f2	P2	
f3	P3	P6 P7

Renaming in practice. The IBM 360/91 had only four floating-point registers (f0–f3), too few to keep its FP pipeline busy. Tomasulo's algorithm (1967) renames each destination to a reservation station entry:

- **Register file:** each entry has a present bit *p* and holds either a value or the tag of the entry that will produce it. Indices map to ISA registers (f0, f1, ...).
- **Reservation stations:** each source operand is a <*p*, tag/data> pair. The tag of an RS entry is the new name for that instruction's result.
- **Common data bus:** a finishing functional unit broadcasts <tag, result>. Every RF and RS entry waiting on that tag copies the result and sets *p*. We call results V0, V1, and so on.

The algorithm:

- **On dispatch** (in program order):
 - Allocate a reservation station (RS) entry. Its ID is the tag.
 - For each source register, if its register file (RF) entry has *p* set, copy the value into the RS and set *p* for that operand. Otherwise, copy the tag from the RF and clear *p*.
 - Write the destination register's RF entry as <*p* = 0, tag>.
- **Before execution:**
 - For missing operands, monitor the result bus for a matching tag. Replace the tag with the value and set *p*.
 - When all operands are present, issue to the functional unit.
- **On completion:**
 - Broadcast <tag, result> on the result bus for the RF and other RS entries to consume.
 - Deallocate the RS entry.

- 1.1 Trace the code below through a Tomasulo machine with three adder reservation stations (T0–T2) feeding a pipelined 2-stage adder, and two multiplier reservation stations (T3–T4) feeding a pipelined 3-stage multiplier. The comments name each instruction's result. Assume:
- At most one instruction dispatches per cycle, in program order, into the lowest-numbered free RS of the right type.
 - An instruction whose operands are all present can issue in the same cycle it dispatches.
 - A result is broadcast in the cycle after its last execute stage. In that cycle, the RF and every waiting RS entry (including one being dispatched) pick it up, the producer's RS entry is freed, and any instruction that is now ready can issue.
 - The bus can broadcast more than one result per cycle.

Fill in the state at the end of each cycle. The initial state is given; the initial value of f1 is never read, so it is left blank.

A: fmul f1, f0, f2 # V3
 B: fadd f0, f3, f1 # V4
 C: fmul f3, f2, f3 # V5
 D: fadd f3, f3, f1 # V6

Cycle 0 Dispatched: –

		p	tag/data	p	tag/data
Adder RS	T0				
	T1				
	T2				
Mult RS	T3				
	T4				

	Stage	Dest tag
Adder	1	
	2	
Mult	1	
	2	
	3	

Reg	p	tag/data
f0	1	V0
f1		
f2	1	V1
f3	1	V2

Cycle 1 Dispatched:

		p	tag/data	p	tag/data
Adder RS	T0				
	T1				
	T2				
Mult RS	T3				
	T4				

	Stage	Dest tag
Adder	1	
	2	
Mult	1	
	2	
	3	

Reg	p	tag/data
f0		
f1		
f2		
f3		

Cycle 2 Dispatched:

		p	tag/data	p	tag/data
Adder RS	T0				
	T1				
	T2				
Mult RS	T3				
	T4				

	Stage	Dest tag
Adder	1	
	2	
Mult	1	
	2	
	3	

Reg	p	tag/data
f0		
f1		
f2		
f3		

Cycle 3 Dispatched:

		p	tag/data	p	tag/data
Adder RS	T0				
	T1				
	T2				
Mult RS	T3				
	T4				

	Stage	Dest tag
Adder	1	
	2	
Mult	1	
	2	
	3	

Reg	p	tag/data
f0		
f1		
f2		
f3		

Cycle 4 Dispatched:

		p	tag/data	p	tag/data
Adder RS	T0				
	T1				
	T2				
Mult RS	T3				
	T4				

	Stage	Dest tag
Adder	1	
	2	
Mult	1	
	2	
	3	

Reg	p	tag/data
f0		
f1		
f2		
f3		

Cycle 5 Dispatched:

		p	tag/data	p	tag/data
Adder RS	T0				
	T1				
	T2				
Mult RS	T3				
	T4				

	Stage	Dest tag
Adder	1	
	2	
Mult	1	
	2	
	3	

Reg	p	tag/data
f0		
f1		
f2		
f3		

Cycle 6 Dispatched:

		p	tag/data	p	tag/data
Adder RS	T0				
	T1				
	T2				
Mult RS	T3				
	T4				

	Stage	Dest tag
Adder	1	
	2	
Mult	1	
	2	
	3	

Reg	p	tag/data
f0		
f1		
f2		
f3		

Cycle 7 Dispatched:

		p	tag/data	p	tag/data
Adder RS	T0				
	T1				
	T2				
Mult RS	T3				
	T4				

	Stage	Dest tag
Adder	1	
	2	
Mult	1	
	2	
	3	

Reg	p	tag/data
f0		
f1		
f2		
f3		

Cycle 8 Dispatched:

		p	tag/data	p	tag/data
Adder RS	T0				
	T1				
	T2				
Mult RS	T3				
	T4				

	Stage	Dest tag
Adder	1	
	2	
Mult	1	
	2	
	3	

Reg	p	tag/data
f0		
f1		
f2		
f3		

- 1.2 Why can't the reservation station entry for an instruction be deallocated immediately on issue?
- 1.3 Why are exceptions *imprecise* in this implementation? Can the current setup support hardware speculation (for example, branch prediction)?

2 Reorder Buffer

To regain precise exceptions and support speculation, the **reorder buffer (ROB)** separates *commit* from *completion*:

- **Completion:** the result is available (out of order).
- **Commit:** architectural state is updated (in order).

	v	i	op	p	rs1/tag	p	rs2/tag	p	result	rd	xcpt?
oldest →											
free →											

Each ROB entry holds a valid bit (v), an issued bit (i), the opcode, present bits and tags or values for both sources and the result, the destination register (rd), and an exception flag. Instructions enter at the free pointer and commit from the oldest pointer.

Terminology. We use the following names for the phases of instruction execution:

Phase	What happens
Fetch	Instruction bits are retrieved from the instruction cache into the fetch buffer.
Decode / rename	Instructions are dispatched into the appropriate issue buffer (ROB / reservation station).
Execute	Instructions and their operands are issued to functional units. When execution completes , all results and exception flags are available.
Commit	The instruction irrevocably updates architectural state, or takes a precise trap. Also called <i>graduation</i> or <i>retirement</i> .

- **Dispatch vs. issue:** dispatch means the instruction is decoded and enters the ROB / reservation station; issue means it is sent to an execution unit. Some papers and diagrams use “issue” for what we call dispatch.
- **Completion vs. commit:** committing in order despite completing out of order is what gives us precise exceptions. “Retired” is also used to mean “committed”.

There are two common ways to organize the ROB and register state:

	Data-in-ROB	Unified physical register file
Uncommitted values	Held in the ROB, which holds both tags and data	Held in the physical register file, alongside committed values
Architectural state	Separate architectural register file, written at commit	A committed register mapping into the physical register file
ROB contents	Tags and data	Only tags

3 Renaming with a Unified Physical Register File

With a unified physical register file (PRF), renaming works as follows:

- **On dispatch**, provide a fresh location for the new result:
 - (a) Allocate a new physical register for the destination from the free list.
 - (b) Update the decode-stage mapping.
- **On commit**, make the mapping “permanent” in the architectural state, and return the old physical register to the pool for reuse. This is why we want in-order commit!
 - (a) Update the architectural mapping.
 - (b) Deallocate the previous physical register for the destination, and add it back to the free list.
- **On exception**, repair the decode-stage rename table by un-renaming in reverse order: walk through the ROB entries from newest to oldest (the [MIPS R10K](#) approach).

3.1 The x registers below are renamed from a pool of physical registers. The free list is a FIFO: a physical register is taken from the head when allocated and added back to the tail when reclaimed. For each instruction, give the physical register assigned as its destination, and the physical register added back to the free list when it commits. Then give the map table after all ten instructions are renamed, and the free list after all ten commit.

Initial map table:

Arch. reg	x1	x2	x3	x4	x5
Phys. reg	p12	p11	p5	p6	p3

Initial free list: head →

p2	p4	p10	p7	p1	p0	p9	p8	p13	p14
----	----	-----	----	----	----	----	----	-----	-----

Instruction	Arch. destination	Phys. destination	To be freed
ld x2, 0(x4)	x2	p2	p11
sw x2, 0(x3)			
addi x4, x4, 0x4			
addi x3, x3, 0x4			
bne x4, x1, loop			
ld x2, 0(x4)			
sw x2, 0(x3)			
addi x4, x4, 0x4			
addi x3, x3, 0x4			
bne x4, x1, loop			

Map table after renaming:

Arch. reg	x1	x2	x3	x4	x5
Phys. reg					

Free list after all ten commit: head →

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- 3.2 Suppose an older instruction A, still in flight, was assigned p11 as its destination, and the first `ld x2, 0(x4)` (call it B) is assigned p2 and will free p11. B finishes executing in 1 cycle, but A takes 100 cycles. When can p11 be added back to the free list? The map table now says x2 maps to p2, so how does A know where to write its result?

- 3.3 Suppose the second load instruction causes an exception. Show the state of the map table and free list just before jumping to the exception handler. Assume the exception is taken when the load reaches the head of the ROB, so all older instructions have committed.

Map table:	Arch. reg	x1	x2	x3	x4	x5
	Phys. reg					

Free list:	head →									
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4 Branch Prediction

Modern processors may have more than 10 pipeline stages between the next PC calculation and branch resolution. Each mispredicted branch costs roughly (pipeline depth from fetch to branch resolution) $\times$ (pipeline width), plus the instructions sitting in buffers such as the fetch queue.

Overall, branches are taken about 60–70% of the time, but backward branches (loops) are taken about 90% of the time, while forward branches are closer to 50%. Dynamic predictors also exploit *correlation* between branch outcomes:

Temporal correlation:

```
for (int i = 0; i < 4; i++)
    sum += i;
```

Spatial correlation:

```
if (x[i] < 7) then
    y += 1;
if (x[i] < 5) then
    c -= 4;
```

Bimodal counters. A 2-bit saturating counter is incremented when the branch is taken and decremented when it is not taken. The upper bit gives the predicted direction.

00	01	10	11
Strongly not taken	Weakly not taken	Weakly taken	Strongly taken

Consider the following code:

```
for (int i = 0; i < 4; i++)    // BRANCH_A (taken = stay in the loop)
    for (int j = 0; j < 4; j++) // BRANCH_B (taken = stay in the loop)
        if (j % 2 != 0)       // BRANCH_C (taken = run the body of the if)
            sum += i;
```

Assume a branch history table (BHT) indexed by PC, and that the PCs of the three branches do not alias into the same entry. In the tables, 1 means taken and 0 means not taken, and the counter is the value before the branch is predicted.

- 4.1 With **1-bit** counters initialized to 0 (not taken), fill in the tables. BRANCH_A is done for you. What is the prediction accuracy for each branch over the whole loop nest?

Branch A:

	$i = 0$	$i = 1$	$i = 2$	$i = 3$	$i = 4$
Counter	0	1	1	1	1
Prediction	0	1	1	1	1
Actual	1	1	1	1	0
Accuracy					

Branch B:

	$j = 0$	$j = 1$	$j = 2$	$j = 3$	$j = 4$	$j = 0$	$j = 1$
Counter							
Prediction							
Actual							
Accuracy							

Branch C:

	$j = 0$	$j = 1$	$j = 2$	$j = 3$	$j = 0$	$j = 1$	...
Counter							...
Prediction							...
Actual							...
Accuracy							

4.2 Repeat with **2-bit** counters initialized to 00 (strongly not taken).

Branch A:

	$i = 0$	$i = 1$	$i = 2$	$i = 3$	$i = 4$
Counter					
Prediction					
Actual					
Accuracy					

Branch B:

	$j = 0$	$j = 1$	$j = 2$	$j = 3$	$j = 4$	$j = 0$	$j = 1$
Counter							
Prediction							
Actual							
Accuracy							

Branch C:

	$j = 0$	$j = 1$	$j = 2$	$j = 3$	$j = 0$	$j = 1$	...
Counter							...
Prediction							...
Actual							...
Accuracy							

Branch history tables. What we just analyzed is a **branch history table (BHT)**: some bits of the PC are used as a hash into a table of counters that store the direction (taken / not taken) of each branch. This captures temporal correlation. Specifically, it is a *single-level* BHT: one table, and no spatial correlation. A 4K-entry BHT with 2 bits per entry predicts about 80–90% of branches correctly.

Two-level predictors also exploit spatial correlation, using the observation that the dynamic behavior of past branches can predict future branches. A **branch history** is a bit vector of taken / not-taken (1 / 0) outcomes, representing both temporal and spatial history. The history is combined with the PC to select a counter. It can be *local* (each branch has its own shift register) or *global* (one shift register shared by all branches).

- 4.3 Consider a two-level predictor, where a branch history selects a prediction from multiple PC-indexed counter tables, running the loop below. Assume no branch aliasing, and that $x[i]$ is random.

```
for (int i = 0; i < N; i++) {    // BRANCH_L (taken = stay in the loop)
    if (x[i] >= 0) pos++;        // BRANCH_1 (taken = run the body)
    if (i % 2 == 0) even++;      // BRANCH_2 (taken = run the body)
    if (x[i] < 0) neg++;         // BRANCH_3 (taken = run the body)
}
```

What is the **minimum** number of history bits needed to predict each branch perfectly? If using local histories, how many local history bits? If using global histories, how many global history bits?

	Local history bits	Global history bits
BRANCH_1		
BRANCH_2		
BRANCH_3		

BHTs vs. BTBs. A BHT provides a direction, but to redirect fetch we need an actual address. That comes from a **branch target buffer (BTB)**: a 2^k -entry table indexed by the PC (direct-mapped, or associative), where each entry holds the branch's PC, a valid bit, and its predicted target PC.

- The next PC is determined before the branch is even fetched and decoded.
- If the PC does not match an entry, PC+4 is fetched.
- Only taken branches and jumps are held in the BTB.

The BTB is consulted in the first fetch stage. The BHT is consulted later, once the instruction is being decoded, and corrects the fetch stream when the BTB misses a predicted-taken branch. Both are only updated after the branch resolves in the execute stage.